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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,207	01/02/2004	Huajie Chen	FIS920030350US1	5359

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/751,207	CHEN ET AL.
	Examiner	Art Unit
	Christy L. Novacek	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed January 2, 2004.

Drawings

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: The appropriate US Patent Application No. needs to be inserted into the first paragraph of page 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-14 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Comita et al. (US 6,774,040).

Regarding claim 1, the admitted prior art discloses performing an ex-situ chemical oxide removal process on a silicon germanium (SiGe) surface so as to remove oxygen from the SiGe surface, thereby leaving a remaining amount of oxygen at the SiGe surface, heating the SiGe surface in a hydrogen bake to remove the remaining amount of oxygen from the SiGe surface, and epitaxially growing an epitaxial silicon-containing layer on the SiGe surface (pg. 4, para. 0017 – pg. 5, para. 0020). The admitted prior art discloses that this oxygen removal process results in a rough SiGe surface. The admitted prior art does not disclose that the hydrogen bake step includes heating the SiGe surface in a chlorine-containing environment. Like the admitted prior art, Comita discloses a method of preparing a semiconductor surface, which may include SiGe, for subsequent silicon epitaxial deposition, wherein the method of preparing the semiconductor surface involves subjecting the surface to a hydrogen bake (col. 1, ln. 35-63; col. 7, ln. 8-25). Comita teaches that by adding HCl and a silane-type gas to the hydrogen bake step, the semiconductor surface can be prepared such that it has the exceptional smoothness that is advantageous in the art (col. 1, ln. 35-63). At the time of the invention, it would have been obvious to one of ordinary skill in the art to add HCl and a silane-type gas to the hydrogen bake step of the admitted prior art because the admitted prior art recognizes that surface roughness is a problem and Comita teaches that by adding the HCl and silane-type gas to the hydrogen bake step, surface roughness can be avoided.

Regarding claims 2 and 12, Comita teaches that by using the H_2/HCl/silane-type gas heating method, the semiconductor surface can be formed such that it has a total RMS value of less than 0.1 nm (1.0 Angstrom).

Regarding claims 3 and 13, the admitted prior art and Comita disclose that the epitaxial silicon-containing layer can be silicon (Si).

Regarding claims 4 and 14, the admitted prior art discloses that the ex-situ chemical oxide removal involves a hydrofluoric acid etch.

Regarding claims 6, 9, 16 and 18, Comita discloses that the chlorine-containing hydrogen bake environment includes a mixture of a larger flow of hydrogen with smaller flows of HCl and dichlorosilane (DCS) (col. 13, ln. 7-25; col. 11, ln. 64 – col. 12, ln. 19).

Regarding claims 7, 8 and 17, Comita discloses that the ratio of HCl and DCS can be varied according to the degree of smoothness desired (col. 3, ln. 49-57; col. 11, ln. 23 – col. 12, ln. 29). At the time of the invention, it would have been obvious to one of ordinary skill in the art to select a ratio of HCl and DCS that provides either a zero or positive etch rate because Comita teaches that the ratio of HCl and DCS can be varied according to the degree of smoothness desired.

Regarding claim 10, the admitted prior art discloses performing an ex-situ chemical oxide removal process on a silicon surface so as to remove oxygen from the silicon surface, thereby leaving a remaining amount of oxygen at the silicon surface, heating the silicon surface in a hydrogen bake to remove the remaining amount of oxygen from the silicon surface, and epitaxially growing an epitaxial silicon-containing layer on the silicon surface (pg. 4, para. 0017 – pg. 5, para. 0020). The admitted prior art discloses that this oxygen removal process results in

a rough silicon surface. The admitted prior art does not disclose that the hydrogen bake step includes heating the silicon surface in a chlorine-containing environment. Like the admitted prior art, Comita discloses a method of preparing a silicon surface for subsequent silicon epitaxial deposition, wherein the method of preparing the silicon surface involves subjecting the surface to a hydrogen bake (col. 1, ln. 35-63; col. 7, ln. 8-25). Comita teaches that by adding HCl and a silane-type gas to the hydrogen bake step, the silicon surface can be prepared such that it has the exceptional smoothness that is advantageous in the art (col. 1, ln. 35-63). At the time of the invention, it would have been obvious to one of ordinary skill in the art to add HCl and a silane-type gas to the hydrogen bake step of the admitted prior art because the admitted prior art recognizes that surface roughness is a problem and Comita teaches that by adding the HCl and silane-type gas to the hydrogen bake step, surface roughness can be avoided.

Regarding claim 11, the admitted prior art does not disclose any particular type of semiconductor substrate or integrated circuit device. Comita teaches that his surface smoothing method is applicable to a SOI substrate. At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the methods taught by the admitted prior art and Comita to any semiconductor substrate or surface on which surface roughness is desired to be smoothed because, as is stated by the admitted prior art, surface roughness is a well-known problem and because strained silicon surfaces and patterned thin silicon-on-insulator substrates are well-known in the art.

Regarding claim 19, the admitted prior art discloses performing an ex-situ chemical oxide removal process on a silicon surface so as to remove oxygen from the silicon surface, thereby leaving a remaining amount of oxygen at the silicon surface, heating the silicon surface in a

hydrogen bake to remove the remaining amount of oxygen from the silicon surface, and epitaxially growing an epitaxial silicon-containing layer on the silicon surface (pg. 4, para. 0017 – pg. 5, para. 0020). The admitted prior art discloses that this oxygen removal process results in a rough silicon surface. The admitted prior art does not disclose that the hydrogen bake step includes heating the silicon surface in a chlorine-containing environment. Like the admitted prior art, Comita discloses a method of preparing a silicon surface for subsequent silicon epitaxial deposition, wherein the method of preparing the silicon surface involves subjecting the surface to a hydrogen bake (col. 1, ln. 35-63; col. 7, ln. 8-25). Comita teaches that by adding HCl and a silane-type gas to the hydrogen bake step, the silicon surface can be prepared such that it has the exceptional smoothness that is advantageous in the art (col. 1, ln. 35-63). At the time of the invention, it would have been obvious to one of ordinary skill in the art to add HCl and a silane-type gas to the hydrogen bake step of the admitted prior art because the admitted prior art recognizes that surface roughness is a problem and Comita teaches that by adding the HCl and silane-type gas to the hydrogen bake step, surface roughness can be avoided. The admitted prior art does not disclose any particular type of semiconductor substrate or integrated circuit device. Comita teaches that his surface smoothing method is applicable to a SOI substrate. At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the methods taught by the admitted prior art and Comita to any semiconductor substrate or surface on which surface roughness is desired to be smoothed because, as is stated by the admitted prior art, surface roughness is a well-known problem and because strained silicon surfaces and patterned thin silicon-on-insulator substrates are well-known in the art.

Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Comita et al. (US 6,774,040), as applied to claims 1 and 10 above, and further in view of Paton et al. (US 6,811,448).

Regarding claims 5 and 15, the admitted prior art does not disclose any particular formulation for the hydrofluoric acid etch. Like the admitted prior art, Paton disclose using a HF etch to remove native oxide from the surface of a semiconductor substrate. Paton teaches that a H_2O:HF solution of anywhere from 50:1 to 1000:1 (col. 4, ln. 22-38). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a H_2O:HF solution of 50:1 to 1000:1 because the admitted prior art does not disclose any particular formulation for the HF etch and Paton discloses that a H_2O:HF ratio of 50:1 to 1000:1 can successfully accomplish the removal of native oxide from a semiconductor substrate.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U'Ren (US 6,514,886) teaches a semiconductor substrate covered by an oxide layer and removing a portion of the oxide layer using a hydrofluoric acid etch and then removing a remainder of the oxide layer using dichlorosilane and hydrochloric acid followed by forming an epitaxial layer on the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
June 8, 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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